Homework 1

(Due date: September 19th @ 5:30 pm)

Presentation and clarity are very important! Show your procedure!

Problem 1 (27 pts)

a) Simplify the following functions using ONLY Boolean Algebra Theorems. For each resulting simplified function, sketch the logic circuit using AND, OR, XOR, and NOT gates. (14 pts)

- ✓ $F(A,B,C) = \prod(M_0, M_1, M_4, M_6)$
- ✓ $F = \overline{x(y \oplus z)} + \bar{y}$
- ✓ $F = (A + \bar{B} + D)(\bar{A}B + \bar{D})$
- ✓ $F = \overline{(\overline{A + B})C + AB\bar{D}}$

b) Determine whether or not the following expression is valid, i.e., whether the left- and right-hand sides represent the same function. Suggestion: complete the truth tables for both sides: (5 pts)

$$x_1x_3 + \overline{x_2}\,\overline{x_3} + \overline{x_1}x_2 = x_2x_3 + \overline{x_1}\,\overline{x_3} + x_1\,\overline{x_2}$$

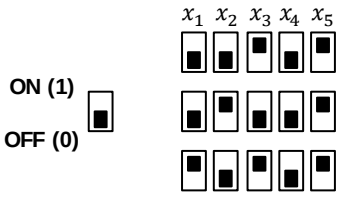
c) For the following Truth table with two outputs: (8 pts)

- Provide the Boolean functions using the Canonical Sum of Products (SOP), and Product of Sums (POS). (4 pts)
- Express the Boolean functions using the minterms and maxterms representations.
- Sketch the logic circuits as Canonical Sum of Products and Product of Sums.

x	y	z	f_1	f_2
0	0	0	1	0
0	0	1	0	1
0	1	0	0	1
0	1	1	0	0
1	0	0	0	1
1	0	1	1	0
1	1	0	0	0
1	1	1	1	0

Problem 2 (18 pts)

a) Security combinations: A lock only opens ($z = 0$) when the 5 switches (x_1, x_2, x_3, x_4, x_5) are set in any of the 3 configurations shown in the figure, otherwise the lock is closed ($z = 1$). A switch generates a '1' in the ON position, and a '0' in the OFF position.



- Provide the simplified Boolean equation for the output z and sketch the logic circuit.

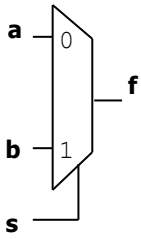
b) A doctoral student is defending his Dissertation. A 4-member committee determines whether to accept or reject the work. A simple majority vote is required. In case of a tie, the outcome is determined by the vote of the chair of the committee.

- Design the circuit (provide the simplified Boolean equation and sketch the logic circuit) that generates $f = 1$ if the committee accepts the work, and $f = 0$ if the work is rejected. We assign x, y, z, w to the vote of each committee member (w is the vote of the chair of the committee), where '1' means accept, and '0' reject. (8 pts)

Problem 3 (13 pts)

a) The following circuit has the following logic function: $f = \bar{s}a + sb$.

- ✓ Complete the truth table of the circuit, and sketch the logic circuit (3 pts)



s	a	b	f
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

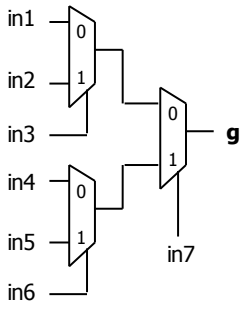
b) We can use several instances of the previous circuit to implement different functions. (10 pts)

- For example, the following selection of inputs produce the function: $g = \overline{x_1}x_2 + x_2x_3$. Demonstrate that this is the case.

in1	in2	in3	in4	in5	in6	in7
0	1	x_2	0	x_3	x_2	x_1

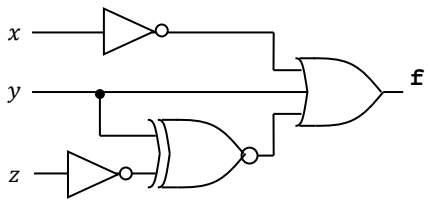
- Given the following inputs, provide the resulting function g (minimize the function).

in1	in2	in3	in4	in5	in6	in7
x_3	0	x_1	1	0	x_1	x_2



PROBLEM 4 (24 PTS)

a) Complete the truth table describing the output of the following circuit and write the simplified Boolean equation (6 pts).

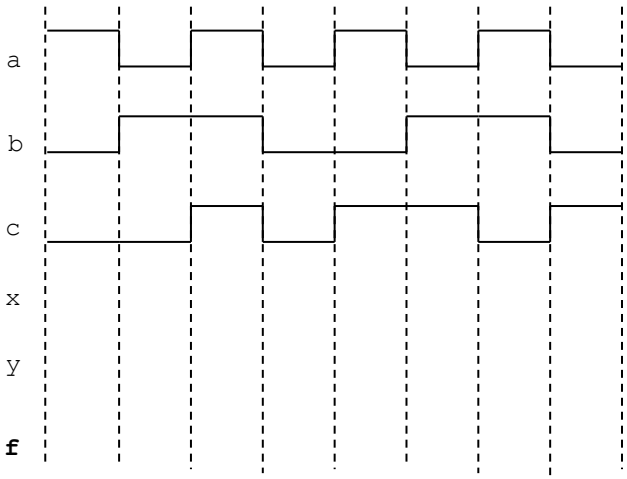


x	y	z	f
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

$f =$

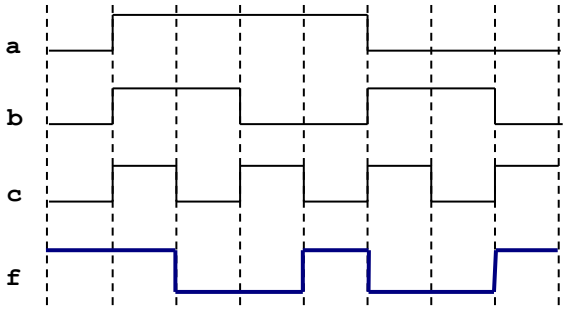
b) Complete the timing diagram of the logic circuit whose VHDL description is shown below: (5 pts)

```
library ieee;
use ieee.std_logic_1164.all;

entity circ is
  port ( a, b, c: in std_logic;
         f: out std_logic);
end circ;

architecture struct of circ is
  signal x, y: std_logic;

begin
  x <= not(a) xor not(c);
  f <= y and (not b);
  y <= x nor b;
end struct;
```

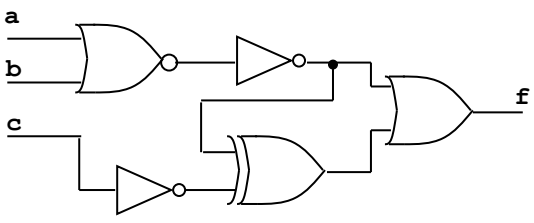


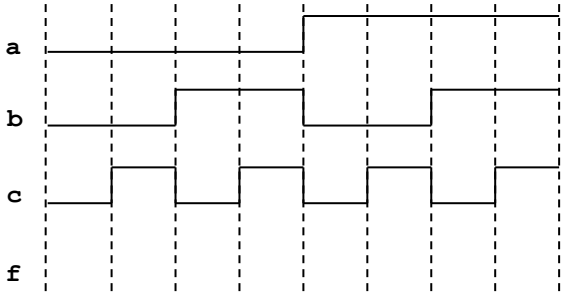
c) The following is the timing diagram of a logic circuit with 3 inputs. Sketch the logic circuit that generates this waveform. Then, complete the VHDL code. (8 pts)

```
library ieee;
use ieee.std_logic_1164.all;

entity wave is
  port ( a, b, c: in std_logic;
               f: out std_logic);
end wave;

architecture struct of wave is
-- ???
begin

   -- ???

end struct;
```



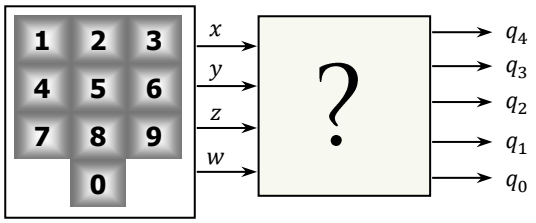
d) Complete the timing diagram of the following circuit: (5 pts)





PROBLEM 5 (18 PTS)

- A numeric keypad produces a 4-bit code $xyzw$ representing an unsigned number from 0 to 9. We want to design a logic circuit that converts each 4-bit code to Morse code (where alphanumeric characters are encoded into sequences of dots and dashes). The figure depicts the Morse code representations for numbers from 0 to 9. The circuit generates 5 bits, where a '0' represents a dot, and '1' represents a dash.



Decimal value	Morse code
0	▬ ▬ ▬ ▬ ▬
1	• ▬ ▬ ▬ ▬
2	• • ▬ ▬ ▬
3	• • • ▬ ▬
4	• • • • ▬
5	• • • • •
6	▬ • • • •
7	▬ ▬ • • •
8	▬ ▬ ▬ • •
9	▬ ▬ ▬ ▬ •

- ✓ Complete the truth table for each output (q_4, q_3, q_2, q_1, q_0). (3 pts)
- ✓ Provide the simplified expression for each output (q_4, q_3, q_2, q_1, q_0). Use Karnaugh maps for q_4, q_3, q_2, and the Quine-McCluskey algorithm for q_1, q_0. Note it is safe to assume that the codes `1010` to `1111` will not be produced by the keypad. (15 pts)

Value	x	y	z	w	q_4	q_3	q_2	q_1	q_0
0	0	0	0	0					
1	0	0	0	1					
2	0	0	1	0					
3	0	0	1	1					
4	0	1	0	0					
5	0	1	0	1					
6	0	1	1	0					
7	0	1	1	1					
8	1	0	0	0					
9	1	0	0	1					
	1	0	1	0					
	1	0	1	1					
	1	1	0	0					
	1	1	0	1					
	1	1	1	0					
	1	1	1	1					